Remarks

Applicants respectfully request reconsideration of this application as amended. Claims 1, 12, 18 and 23 have been amended. No claims have been cancelled. Therefore, claims 1-26 are presented for examination.

Claims 1-26 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,292,872) in view of the standard practice of integrating circuits, as further evidenced by Sherburne (U.S. Pub. No. 2002/0184546). Applicants submit that the present claims are patentable over the combination of Arimilli and Sherburne.

Arimilli discloses a process wherein if a read request misses in both an L1 cache 12a and an L2 cache 14a, a cache controller 36 of L2 cache 14a presents the read request as a transaction on interconnect 16, which is snooped by each of L2 caches 14b-14n as well as by L3 cache 15a. In response to snooping the read request on interconnect 16, cache controller 36 in each of L2 caches 14b-14n determines if the requested data is resident in its data array 34 or the associated one of L1 caches 12b-12n. See Arimilli at col. 6, ll. 11-18. If the data requested by processor 10a is not resident in L1 cache 12a, L2 cache 14a, or L3 cache 15a, but is stored, for example, in L1 cache 12n in M state 80, cache controller 36 of L2 cache 14n responds to the read request with a modified response and signals L1 cache 12n to push the requested data to L2 cache 14n. Thereafter, L2 cache 14n sources the requested data on interconnect 16 (col. 6, ll. 35-41).

Sherburne discloses a low power configurable processor core. See Sherburne at Abstract.

Claim 1 of the present application recites control logic coupled to first and second dedicated caches to receive a first cache line directly from the first dedicated cache and to

transfer the first cache line directly to the second dedicated cache. Applicants submit that neither Arimilli nor Sherburne disclose or suggest transferring a cache line directly between a first dedicated processor cache to a second dedicated processor cache via control logic. Instead, Arimilli discloses push data from a first L1 cache pushes data to a first L2 cache on to an interconnect, to a second L2 cache and finally a second L1 cache, if the second L1 cache does not contain the data. Thus, Arimilli does not disclose or suggest transferring a cache line directly between a first dedicated processor cache to a second dedicated processor cache via control logic.

Since neither Arimilli nor Sherburne disclose or suggest transferring a cache line from a first dedicated processor cache and to transfer the first cache line to a second dedicated processor cache, any combination of Arimilli and Sherburne would not disclose or suggest such a feature. Thus, claim 1 is patentable over Arimilli in view of Sherburne. Claims 2-11 depend from claim 1 and include additional features. Therefore, claims 2-11 are also patentable over Arimilli in view of Sherburne.

Claim 12 recites transferring a first cache line directly from a first dedicated cache of a chip multi-processor to control logic in the chip multi-processor and subsequently transferring the first cache line from the control logic directly to a second dedicated cache of the chip multi-processor. For the reasons described above with respect to clam 1, claim 12 is also patentable over Arimilli in view of Sherburne. Because claims 13-17 depend from claim 12 and include additional features, claims 13-17 are also patentable over Arimilli in view of Sherburne.

Claim 18 recites control logic coupled to first and second dedicated caches to receive a first cache line directly from the first dedicated cache and to transfer the first cache line

directly to the second dedicated cache. Thus, for the reasons described above with respect to clam 1, claim 18 is also patentable over Arimilli in view of Sherburne. Since claims 19-22 depend from claim 12 and include additional features, claims 13-17 are also patentable over Arimilli in view of Sherburne.

Claim 22 recites transferring a first cache line directly from a first dedicated cache of a chip multi-processor to control logic in the chip multi-processor and subsequently transferring the first cache line from the control logic directly to a second dedicated cache of the chip multi-processor. For the reasons described above with respect to clam 1, claim 22 is also patentable over Arimilli in view of Sherburne. Because claims 23-26 depend from claim 12 and include additional features, claims 23-26 are also patentable over Arimilli in view of Sherburne.

As discussed above, neither Arimilli nor Sherburne disclose or suggest transferring a cache line from. Arimilli discloses an architecture having dedicated processor caches. However, there is no disclosure of control logic that transfers cache lines between the dedicated processor caches.

Applicants respectfully submit that the rejections have been overcome and that the claims are in condition for allowance. Accordingly, applicants respectfully request the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Applicants respectfully petition for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our

Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17(a) for such an extension.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: January 24, 2006

Mark L. Watson
Reg. No. 46,322

12400 Wilshire Boulevard
7th Floor
Los Angeles, California 90025-1026
(303) 740-1980